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EXPRESS MAIL RECEIPT
NUMBER: EL046221547US
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Mary Paul
Signature

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

RE: *U.S. Patent Application Entitled: AND ADVANCED ISOLATION STRUCTURE FOR HIGH DENSITY SEMICONDUCTOR DEVICES AND METHOD FOR MAKING SAME – Mark I. Gardner and Mark C. Gilmer (TT2587)*

Sir:

Transmitted herewith for filing are:

(1) 19-page patent specification with 28 claims and an abstract (also Figures 1-5 on 3 sheets);
(2) Declaration;
(3) Power of Attorney; and,
(4) Assignment and Assignment Cover Sheet.

All correspondence, notices, official letters and other communications should be directed to J. Mike Amerson, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, TX 77040, and that all telephone calls be directed to J. Mike Amerson at (713) 934-4055.

The Assistant Commissioner is authorized to deduct the amount of the total filing fee (listed below) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT2546.

*Patent Agent

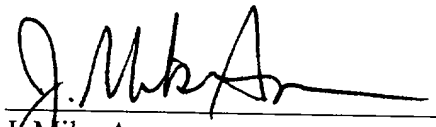
FILING FEE CALCULATION

FOR		Small Entity	Large Entity
Total Claims	28 - 20 = 8	x $11 = $	or x $22 = $ 176.00
Independent Claims	5 - 3 = 2	x $41 = $	or x $82 = $ 164.00
Multiple Dependent Claim(s)		+ $135 = $	or + $270 = $ 0.00
Basic Fee:		+ $395 = $	or + $790 = $ 790.00
Assignment Recording Fee:	($40 per assignee)	+ = $	+ = $ 40.00
TOTAL FILING FEES		**$ 0.00**	**$1,170.00**

Pursuant to 37 C.F.R. § 1.10 the Applicant requests the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail.

Please date stamp and return the enclosed postcards to evidence receipt of these materials.

Respectfully submitted,



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Enclosures

2000.002600
TT2587

Application for United States Letters Patent

for

AN ADVANCED ISOLATION STRUCTURE FOR HIGH DENSITY SEMICONDUCTOR DEVICES AND METHOD FOR MAKING SAME

by

Mark I. Gardner
Mark C. Gilmer

EXPRESS MAIL MAILING LABEL

NUMBER EL046221547US

DATE OF DEPOSIT 5-15-98

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Mary Paul
Signature

AN ADVANCED ISOLATION STRUCTURE FOR HIGH DENSITY SEMICONDUCTOR DEVICES AND METHOD FOR MAKING SAME

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

This invention generally relates to semiconductor processing, and, more particularly, to the isolation of transistors formed on a substrate.

2. DESCRIPTION OF THE RELATED ART

The implementation of electrical circuits requires connecting isolated devices through very specific electrical paths. As it relates to the fabrication of various integrated circuits on, for example, a silicon substrate, this means that the various devices formed in the silicon must be electrically isolated from one another. Such devices, when properly isolated, may thereafter be interconnected to create specific electrical circuits.

The ability to effectively isolate electrical devices, such as transistors, from one another is very important in the fabrication of integrated circuits. For example, effective isolation of electrical field effect transistors is highly desirable to prevent the establishment of unwanted parasitic channels between adjacent devices. Yet another example is the requirement for effective isolation of the collector regions of bipolar integrated circuits.

Generally speaking, the deeper an isolation structure extends into the surface of the substrate, the better the performance of the isolation structure. However, problems have been

encountered as the depth of single width trenches has been increased. For example, with deep, single width trenches, problems have arisen at the intersection of the trench with the surface of the substrate. The problems have included, but are not limited to, lack of adhesion of process layers on the surface of the substrate, cracks in the substrate and/or the process layers, and delamination of process layers, etc.

The present invention is directed to a method and device that solves some or all of the aforementioned problems.

SUMMARY OF THE INVENTION

The present invention is directed to a semiconductor device having an improved structure for isolating transistors formed on a semiconductor substrate, and a method for making same. The device is comprised of a semiconductor device having a first recess formed in the substrate of the device. The first recess has a first width and extends a first depth beneath the surface of the substrate. The device further comprises a second recess formed in the substrate of the device. The second recess has a second width and extends a second depth beneath the surface of the substrate. The second depth of the second recess is greater than the first depth of the first recess, and the first width of the first recess is greater than the second width of the second recess. The device further comprises an isolation structure positioned in at least a portion of the first and second recesses.

The inventive method disclosed herein comprises forming a first recess in the substrate of the device, said first recess having a first depth and a first width, and forming a second recess in

the substrate of the device, the second recess having a second depth and a second width. The first width of the first recess is formed such that it is greater than the second width of the second recess, and the second depth of the second recess is formed such that it is greater than the first depth of the first recess. The method further includes formation of an isolation structure in the first and second recesses.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a cross-sectional view showing formation of an initial trench of the present invention;

Figure 2 is a cross-sectional view showing formation of a plurality of spacers in the initial trench of the present invention;

Figure 3 is a cross-sectional view showing formation of a second trench of the present invention;

Figure 4 is a cross-sectional view showing formation of an isolation material in the second trench of the present invention; and

Figure 5 is a cross-sectional view showing an advanced isolation region of the present invention.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The invention disclosed herein will now be described with reference to Figures 1-5. As shown in Figure 1, a masking layer 10 is formed on a substrate 12. A layer of photoresist 14 is formed on the masking layer 10. The photoresist layer 14 is patterned to define an opening 16.

Thereafter, the portion of the masking layer 10 within the opening 16 is removed and an initial trench 18 is formed in the substrate 12. The initial trench 18 has a bottom 28 and sidewalls 21. The sidewalls 21 of the initial trench 18 may be formed at an angle ranging between 80-90° relative to the surface 20 of the substrate 12.

The masking layer 10 may be formed from a variety of materials, including, but not limited to, oxide, nitride, oxynitride, etc. As readily recognized by those skilled in the art, the masking layer 10 may be formed by a variety of techniques, including, but not limited to, deposition, thermal growing, sputtering, etc. In one embodiment, the masking layer 10 is oxynitride, which may range between 50-100 Å in thickness. The substrate 12 may be made of any semiconductor material, and, in one embodiment, the substrate 12 is doped silicon.

The masking layer 10 may be removed at the same time that the initial trench 18 is formed in the substrate 12. Alternatively, the masking layer 10 may be removed in a separate process step, for example, a wet etch step, prior to the formation of the initial trench 18. In one embodiment, the masking layer 10 is removed and the initial trench 18 is formed during a single process step. For example, the masking layer 10 may be removed and the initial trench 18 may be formed by a plasma etch or reactive ion etch process using, for example, HBr and Cl_2 as the etchant gases. Those skilled in the art will recognize that the particular etch chemistry used will depend upon design conditions. In one embodiment, the initial trench 18 may be approximately 2000-3000 Å wide and may extend beneath the surface 20 of the substrate 12 by approximately 500-1000 Å.

As shown in Figure 2, the photoresist layer 14 is removed. A spacer material is then deposited into the initial trench 18 and onto at least a portion of the surface 22 of the masking layer 10. Thereafter, an anisotropic etch is performed that results in the formation of spacers 24 as shown in Figure 2. By way of example only, the spacers 24 may be formed by a plasma etch process using $ArCHF_3$ and $ArCF_4$ as the etchant gases. Of course, other etch chemistries may be used.

The spacers 24 may be made from a variety of materials, such as oxide, oxynitride, nitride, etc. In one embodiment, the spacers 24 may be made of oxide and may have a thickness ranging between approximately 300-1000 Å. It is desirable that the spacers 24 be made of a material other than the material used to make the masking layer 10, to allow for subsequent selective removal of the masking layer 10 without removing the spacers 24 (as discussed more fully below).

With reference to Figure 3, the next process involves forming a second trench 26 having a bottom 32 and sidewalls 34 in the substrate 12. The sidewalls 34 of the second trench 26 may be formed at an angle ranging between 80-90° relative to the surface 20 of the substrate 12. The second trench 26 may be formed using the same processes (discussed above) used to form the initial trench 18, *e.g.*, plasma etching or reactive ion etching. In one embodiment, the second trench 26 may have a width ranging between approximately 1000-2400 Å and may extend approximately 1000-3000 Å below the bottom 28 of the initial trench 18. Stated in the alternative, the second trench 26 would extend approximately 1500-4000 Å beneath the surface 20 of the substrate 12.

As shown in Figure 4, the next process involves forming an isolation liner 30 in the second trench 26. The isolation liner 30 may extend across the bottom 32 and sides 34 of the second trench 26 formed in the substrate 12, as well as along the sidewalls 36 of the spacers 24. Thereafter, an isolation material 40 may be formed in the area defined by the second trench 26 and the sidewalls 36 of the spacers 24. In one embodiment, the isolation liner 30 is positioned between the spacers 24 and the isolation material 40. Of course, the isolation liner 30 may be omitted or only deposited on portions of the surfaces depicted in Figure 4.

As is apparent to those skilled in the art, the material or materials selected to be deposited in the combined area defined by the initial trench 18 and the second trench 26 may be considered to be an isolation structure 46. The particular material or materials used to form the isolation structure 46 will vary depending upon design requirements. For example, the isolation structure 46 could be comprised of a single material that would fill the entire region defined by the initial trench 18 and the second trench 26. Alternatively, the isolation structure 46 may be comprised of multiple materials positioned within the initial trench 18 or second trench 26, or portions thereof, as dictated by design or manufacturing considerations.

One illustrative embodiment of an isolation structure 46 is shown in Figures 4 and 5. As depicted therein, the isolation structure 46 may be comprised of the spacers 24, isolation liner 30 and isolation material 40. However, the illustrative embodiment of an isolation structure 46 shown in Figure 5 should not be construed as a limitation of the present invention. To the contrary, those skilled in the art will readily recognize that the materials selected for the isolation

structure 46 and the particular configuration of those materials with the initial trench 18 and the second trench 26 are purely a matter of design choice.

The isolation liner 30 may be formed from a variety of materials, including, but not limited to, oxide, oxynitride, nitride, tetraethyl orthosilicate ("TEOS"), etc. In one embodiment, the isolation liner 30 may be made of TEOS and may be approximately 50-150 Å thick. As will be readily recognized by those skilled in the art, the isolation liner 30 may be formed by a variety of techniques, including, but not limited to, chemical vapor deposition and sputtering.

The isolation material 40 may be comprised of any of a variety of materials having a low dielectric constant ("k"), such as fluorosilicate glass, silicon oxyfluoride, hydrogen silsesquixane, fluorinated polyslicon, poly-phenylquinoxaline, polyquinoline (k=3.0), methylsilsesquixane polymer, and fluoro-polymide. The isolation material 40 may have a dielectric constant ranging between 2.5-3.5. The isolation material 40 may be formed by a variety of techniques, including, but not limited to, deposition, sputtering and spinning the material on the substrate. In one embodiment, the isolation material 40 may be polyquinoline, with a "k" value of approximately 3.0, that is formed by spinning the material on the substrate.

After the isolation liner 30 and the isolation material 40 are formed, the wafer is polished, for example, by a chemical mechanical polishing process, to remove any excess material used to form the isolation liner 30 and isolation material 40, and to planerize the isolation material 40, isolation liner 30 and spacers 24 with the surface 22 of the masking layer 10. Thereafter, as

shown in Figure 5, the masking layer 10 may be removed and transistors 42 and 44 (shown schematically) may be formed using traditional techniques.

The advanced isolation structure and technique disclosed herein provides effective isolation of semiconductor devices formed on a substrate. In particular, the formation of an isolation structure involving a dual depth, dual width trench reduces or eliminates some of the problems traditionally encountered at the intersection of a deep, single width trench and the surface of the substrate. This is accomplished by the formation of an initial trench 18 to a depth that is shallower than the depth of traditional deep, single width trenches. Additionally, the configuration of the dual depth, dual width trench disclosed herein may allow for the formation of more effective isolation structures 46. For example, and by way of illustration only, an isolation material 40 having a low "k" value may be used as part of the overall isolation structure 46. This isolation material 40 may be isolated from the substrate 12 by, for example, a liner 30. This liner 30 acts to prevent the low "k" isolation material 40 from contaminating the substrate 12. In one embodiment, the spacers 24 act to insulate the isolation material 40 from parts of adjacent semiconductor devices, such as source and drain regions. However, as discussed above, the particular isolation structure 46 depicted in the drawings is illustrative only, and does not represent the only isolation structure 46 that can be made using the disclosed trench configurations and technologies.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. Furthermore, no limitations are intended to the details

of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

Doc Code: AP.PRE.REQ

CLAIMS

WHAT IS CLAIMED:

1. A semiconductor device, comprising:

a substrate, said substrate having a surface;

a first recess and a second recess formed in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate, said second recess having a second width and extending a second depth beneath the surface of said substrate;

said first width of said first recess being greater than said second width of said second recess;

said second depth of said second recess being greater than said first depth of said first recess; and

an isolation structure positioned in at least a portion of said first and second recesses.

2. The device of claim 1, wherein said isolation structure is comprised of a single isolation material.

3. The device of claim 1, wherein said isolation structure is comprised of a plurality of spacers formed in said first recess.

4. The device of claim 1, wherein said isolation structure is comprised of an isolation liner positioned in at least a portion of at least one of said first and second recesses.

5. The device of claim 1, wherein said isolation structure is comprised of:

a plurality of spacers positioned in said first recess;

an isolation liner positioned in at least a portion of said second recess; and

an isolation material positioned between said spacers and in said second recess adjacent said isolation liner.

6. The device of claim 1, wherein said isolation structure comprises:

a plurality of spacers positioned in said first recess;

an isolation liner positioned in said second recess and extending between said spacers; and

an isolation material positioned in said first and second recesses between said isolation liner.

7. The device of claim 1, wherein said isolation structure is comprised of silicon dioxide.

8. The device of claim 1, wherein said isolation structure is comprised of oxynitride.

9. The device of claim 3, wherein said spacers are oxide spacers.

10. The device of claim 3, wherein at least one of said spacers is an oxynitride spacers.

11. The device of claim 4, wherein said isolation liner is comprised of at least one of the group of tetraethyl orthosilicate, oxide, oxynitride or nitride.

12. The device of claim 1, wherein said first depth of said first recess ranges between approximately 500-1000 Å beneath the surface of said substrate.

13. The device of claim 1, wherein said second depth of said second recess extends approximately 1500-4000 Å beneath the surface of said substrate.

14. The device of claim 2, wherein said first width of said first recess ranges between 2000-3000 Å.

15. The device of claim 2, wherein said second width of said second recess ranges between 1400-2000 Å.

16. A semiconductor device, comprising:

a substrate, said substrate having a surface;

a first recess and a second recess formed in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate, said second recess having a second width and extending a second depth beneath the surface of said substrate;

said first width of said first recess being greater than said second width of said second recess;

said second depth of said second recess being greater than said first depth of said first recess; and

an isolation material positioned in at least a portion of said first and second recesses.

17. The device of claim 16, further comprising a plurality of spacers positioned in said first recess.

18. The device of claim 16, further comprising an isolation liner positioned in at least a portion of said second recess, at least a portion of said isolation liner positioned between said spacers and said isolation material.

19. A semiconductor device, comprising:

a substrate, said substrate having a surface;

a first recess and a second recess formed in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate, said second recess having a second width and extending a second depth beneath the surface of said substrate;

said first width of said first recess being greater than said second width of said second recess;

said second depth of said second recess being greater than said first depth of said first recess; and

an isolation structure, said isolation structure comprising:

a plurality of spacers positioned in said first recess;

an isolation liner positioned in said second recess and adjacent said spacers; and

an isolation material positioned in said first and second recess, said isolation material being positioned adjacent said isolation liner.

20. A method for forming an isolation trench in a semiconductor substrate, said substrate having a surface, comprising:

forming a first recess in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate;

forming a second recess in said substrate, said second recess having a second width that is less than said first width of said first recess, said second recess extending a second depth beneath the surface of said substrate, said second depth being greater than said first depth of said first recess; and

forming an isolation structure in said first and second recesses.

21. The method of claim 20, wherein forming an isolation structure comprises forming at least one material in at least one of said first and second recesses.

22. The method of claim 20, wherein forming an isolation structure comprises forming a single material in said first and second recesses.

23. The method of claim 20, wherein forming an isolation structure comprises forming at least two different materials.

24. The method of claim 20, wherein forming said isolation structure comprises:

forming a plurality of spacers in said first recess;

forming an isolation liner in at least a portion of said second recess; and

forming an isolation material in said second recess adjacent said isolation liner, at least a portion of said isolation liner extending between said spacers and said isolation material.

25. The method of claim 20, wherein forming a first recess comprises etching said first recess.

26. The method of claim 20, wherein forming said second recess comprises etching said second recess.

27. The method of claim 20, wherein forming an isolation material comprises depositing said isolation material in said second recess.

28. A method for forming an isolation trench in a semiconductor substrate, said substrate having a surface, comprising:

forming a first recess in said substrate, said first recess having a first width and extending a first depth beneath the surface of said substrate;

forming a second recess in said substrate, said second recess having a second width that is less than said first width of said first recess, said second recess extending a second depth beneath the surface of said substrate, said second depth being greater than said first depth of said first recess;

forming a plurality of spacers in said first recess;

forming an isolation liner in at least a portion of said second recess; and

forming an isolation material in said second recess adjacent said isolation liner, at least a portion of said isolation liner extending between said spacers and said isolation material.

ABSTRACT OF THE DISCLOSURE

The present invention is directed to a semiconductor device having an improved structure for isolating transistors formed on a semiconductor substrate, and a method for making same. The device is comprised of a semiconductor device having first and second recesses formed in the substrate of the device. The inventive method disclosed herein comprises forming first and second recesses in the substrate of the device. The first width of the first recess is formed such that it is greater than the second width of the second recess, and the second depth of the second recess is formed such that it is greater than the first depth of the first recess.

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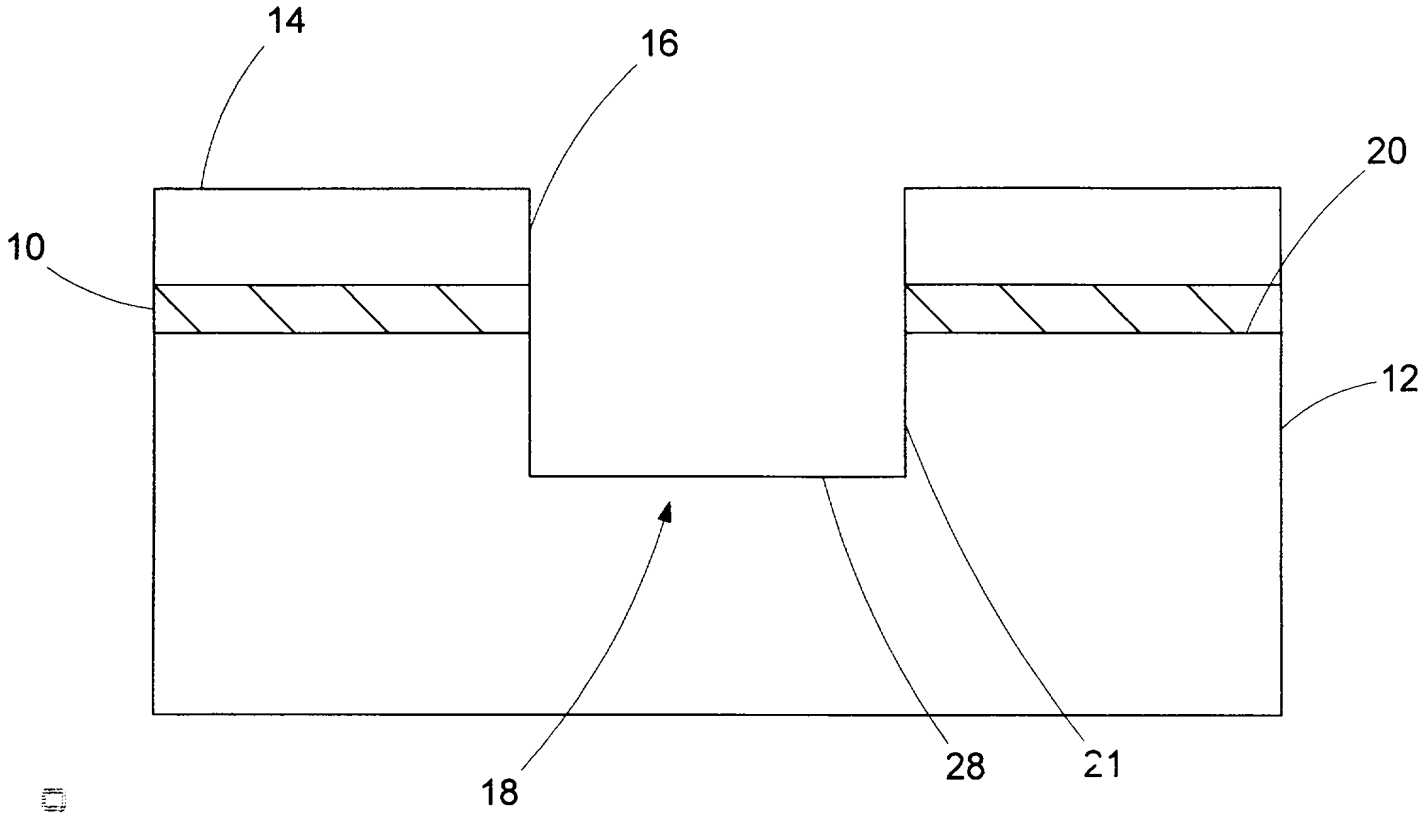

FIG. 1

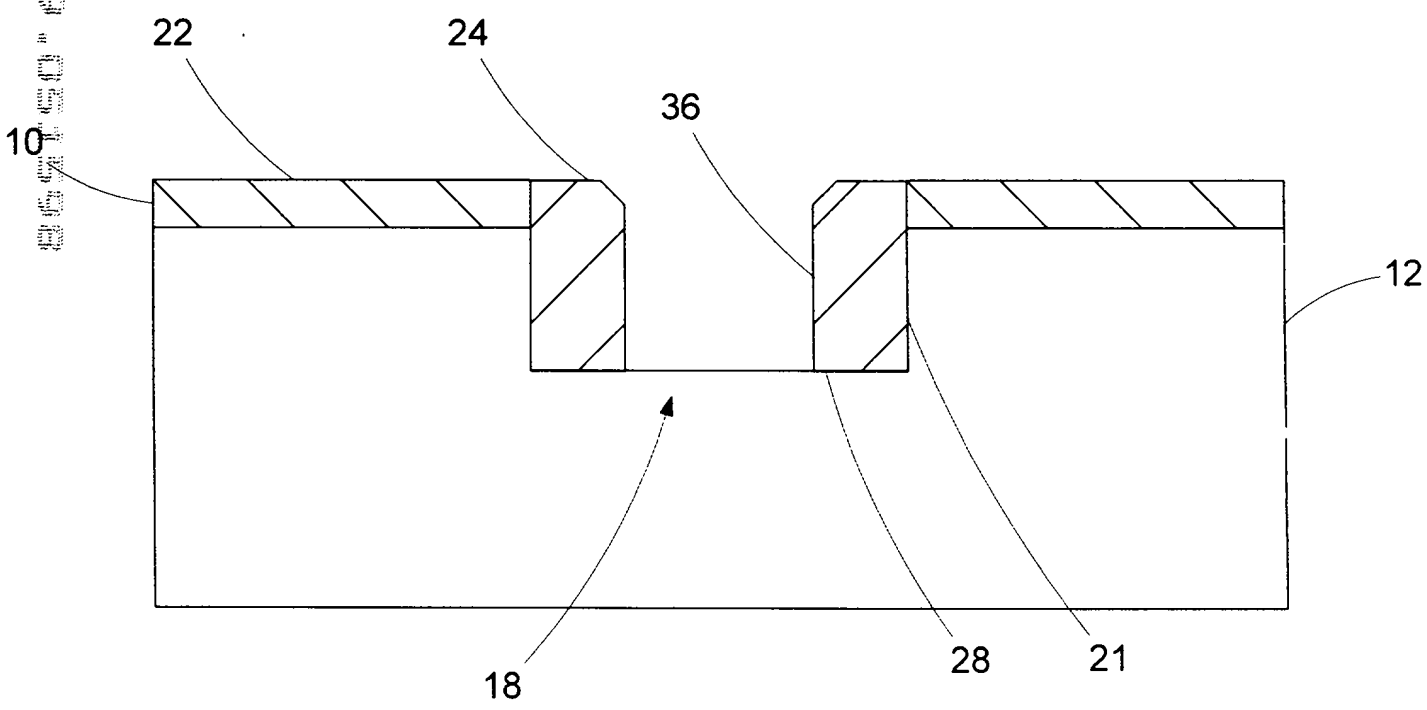

FIG. 2

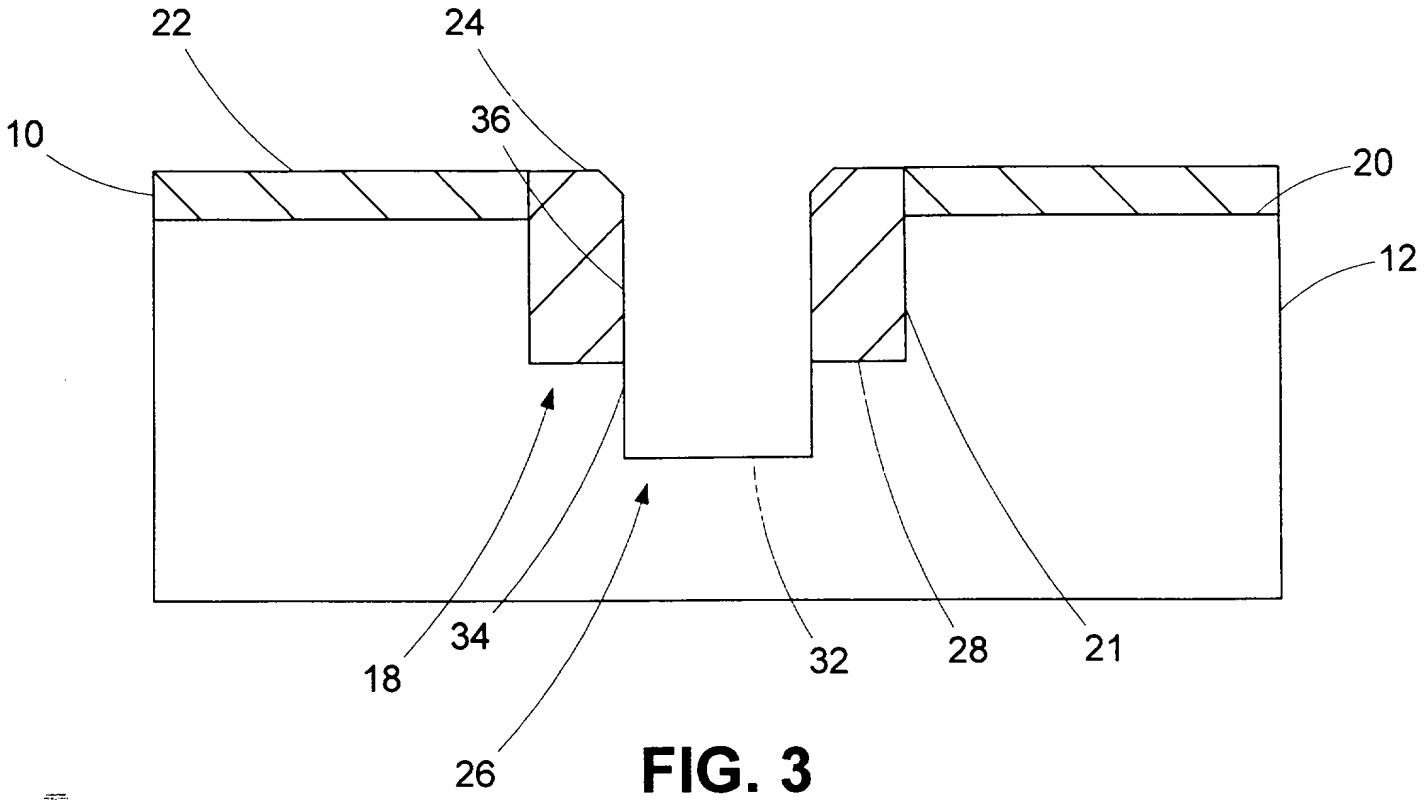
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FIG. 3

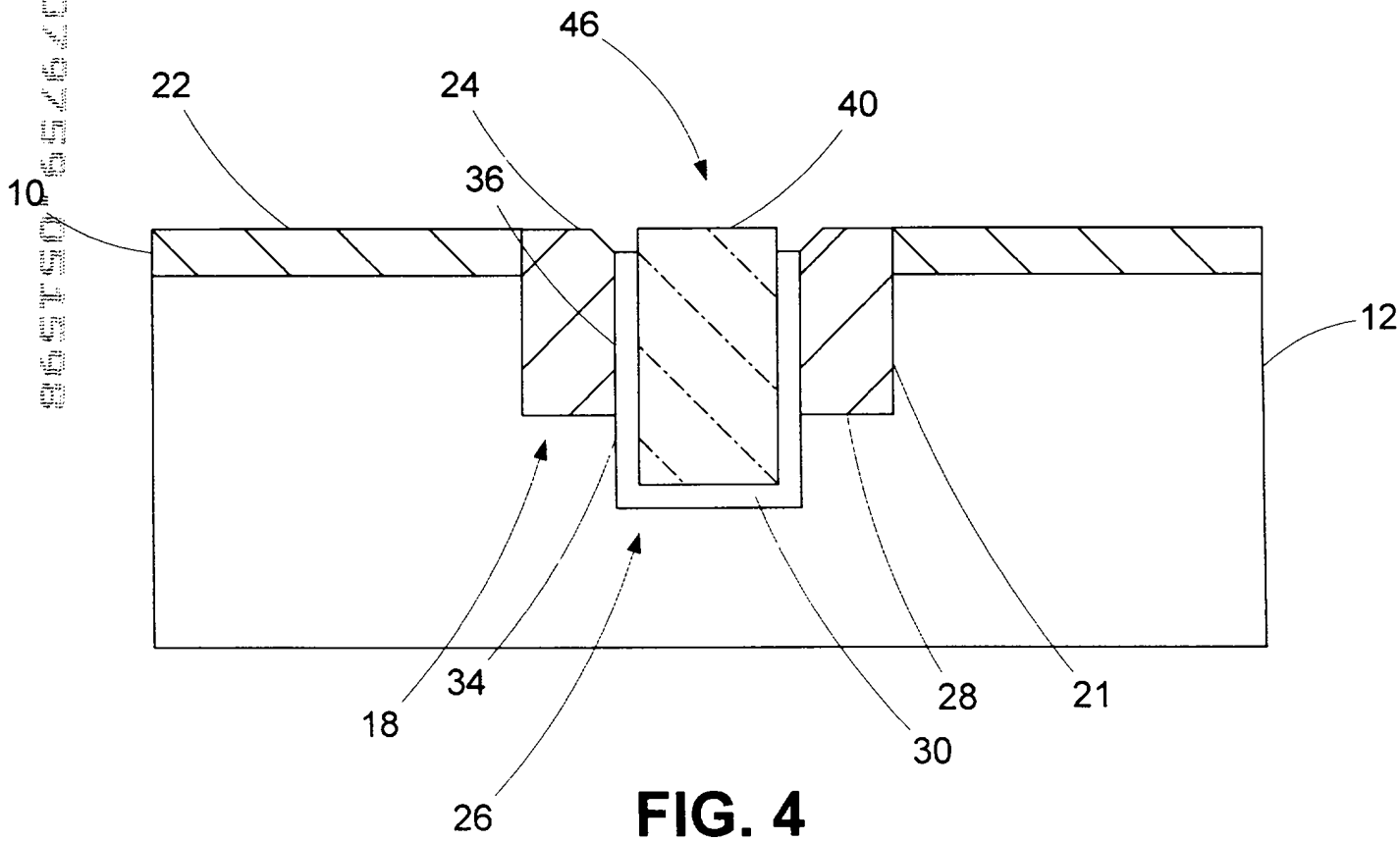
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FIG. 4

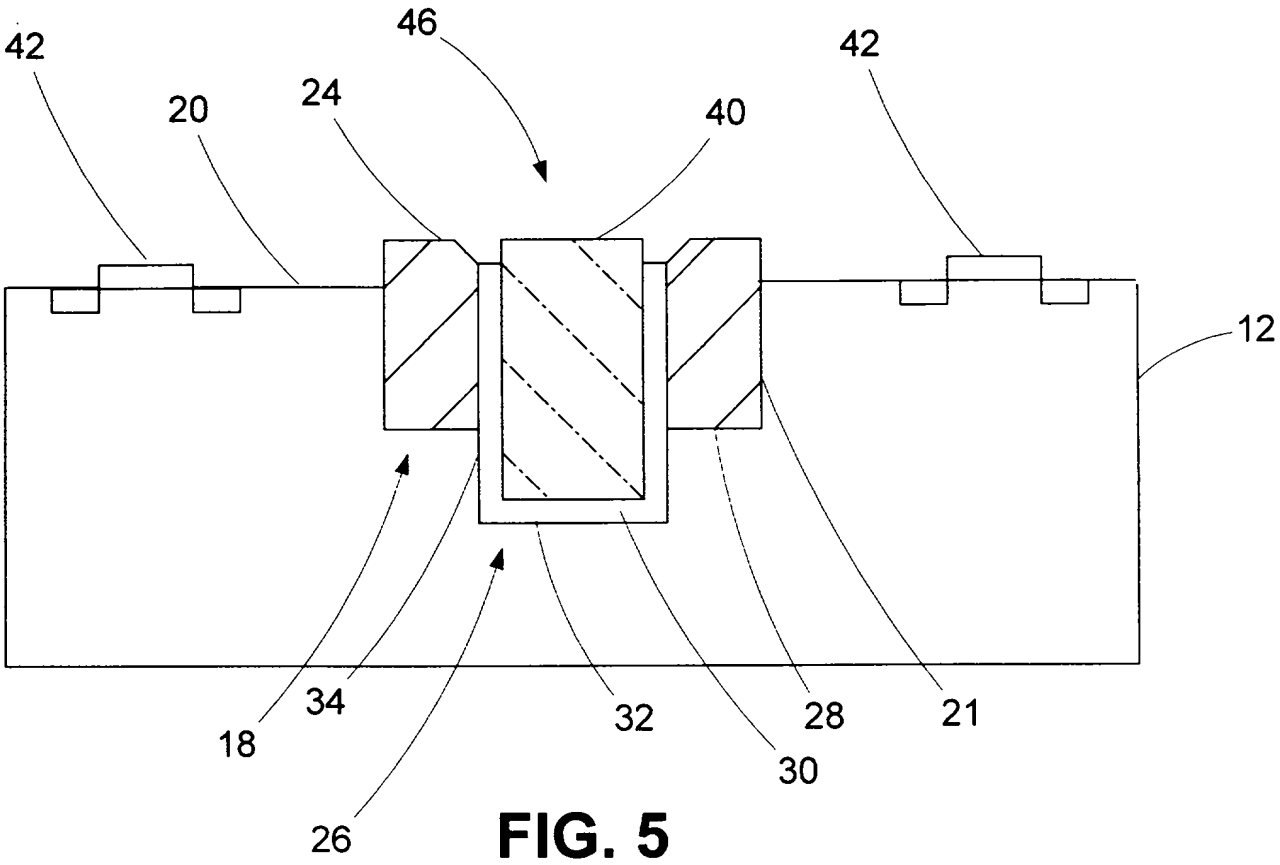

FIG. 5

PATENT
FILE NO. 2000.002600/TT2587

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or the below named inventors are the original, first and joint inventors (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **"AN ADVANCED ISOLATION STRUCTURE FOR HIGH DENSITY SEMICONDUCTOR DEVICES AND METHOD FOR MAKING SAME,"** the Specification of which:

☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent, United States provisional application(s), or inventor's certificate listed below and have also identified below any foreign application for patent, United States provisional application, or inventor's certificate having a filing date before that of the application on which priority is claimed:

PRIORITY APPLICATION(S)			Priority Claimed
(Number)	(Country)	(Date Filed)	Yes/No
(Number)	(Country)	(Date Filed)	Yes/No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56, which become available between the filing date of the prior application and the national or PCT international filing date of this application:

(Application Serial No.)	(Filing Date)	(Status)
(Application Serial No.)	(Filing Date)	(Status)

I hereby direct that all correspondence and telephone calls be addressed to J. Mike Amerson. Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, Texas 77040, (713) 934-7000.

I HEREBY DECLARE THAT ALL STATEMENTS MADE OF MY OWN KNOWLEDGE ARE TRUE AND THAT ALL STATEMENTS MADE ON INFORMATION AND BELIEF ARE BELIEVED TO BE TRUE; AND FURTHER THAT THESE STATEMENTS WERE MADE WITH THE KNOWLEDGE THAT WILLFUL FALSE STATEMENTS AND THE LIKE SO MADE ARE PUNISHABLE BY FINE OR IMPRISONMENT, OR BOTH, UNDER SECTION 1001 OF TITLE 18 OF THE UNITED STATES CODE AND THAT SUCH WILLFUL FALSE STATEMENTS MAY JEOPARDIZE THE VALIDITY OF THE APPLICATION OR ANY PATENT ISSUED THEREON.

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Country of Citizenship:	U.S.A. Date: 5/14/98
Residence Address: (street, number, city, state, and/or country)	12311 Shropshire Boulevard Austin, Texas 78753
Post Office Address: (if different from above)	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:	§	
MARK I. GARDNER	§	
MARK C. GILMER	§	Examiner: Unknown
	§	
Serial No.: Unknown	§	Group Art Unit: Unknown
	§	
Filed: Concurrently Herewith	§	Att'y Docket: 2000.002600/TT2587
	§	
For: AN ADVANCED ISOLATION	§	
STRUCTURE FOR HIGH DENSITY	§	
SEMICONDUCTOR DEVICES AND	§	
METHOD FOR MAKING SAME	§	

POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, being the inventors named in the above-identified application, hereby revoke any previous Powers of Attorney and appoint:

Paul S. Drake, Reg. No. 33,491; J. Vincent Tortolano, Reg. No. 31,433; Louise K. Miller, Reg. No. 36,609; Elizabeth A. Apperley, Reg. No. 36,428; Vincenzo D. Pitruzella, Reg. No. 28,656 Louis A. Riley, Reg. No. 39,817; Rita M. Wisor, Reg. No. 41,382; Charles Quarton, Reg. No. 24,825; and Richard J. Roddy, Reg. No. 27,688; of Advanced Micro Devices, Inc.; and

Danny L, Williams, Reg. No. 31,892; Terry D. Morgan, Reg. No, 31,181; J. Mike Amerson, Reg. No. 35,426; Scott F. Diring, Reg. No. 35,119; of Williams, Morgan & Amerson;

as its attorney or agent so long as they remain with such firms, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Please direct all communications as follows:

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Signature: Mark I. Gardner Date: 5/14/98
Mark I. Gardner

Signature: Mark C. Gilmer Date: 5/14/98
Mark C. Gilmer